

1        CLAIMS

2        What is claimed is:

3        1. Structure comprising:

4              a printed circuit board containing a plurality of  
5              component contacts for receipt of electronic  
6              components;

7              a plurality of electrically conductive traces  
8              formed on said printed circuit board, each trace being  
9              electrically connected to a corresponding one of said  
10             component contacts; and

11             at least one integrated circuit mounted on a  
12             selected portion of said printed circuit board and  
13             containing a plurality of conductive leads, each of  
14             said conductive leads being electrically connected to a  
15             corresponding one of said electrically conductive  
16             traces formed on said printed circuit board thereby to  
17             form an electrically conductive path from each of said  
18             conductive contacts to the corresponding conductive  
19             leads on said at least one integrated circuit, said at  
20             least one integrated circuit being configurable by a  
21             user to interconnect selected electrically conductive  
22             traces on said printed circuit board to achieve a  
23             desired electrical function from the electronic  
24             components to be connected to said printed circuit  
25             board.

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27        2. Structure as in Claim 1 wherein said printed  
28             circuit board contains more than one layer of conductive  
29             traces.

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31        3. Structure as in Claim 1 wherein at least some of  
32             said plurality of electrical contacts comprise a plurality  
33             of holes in said printed circuit board, each hole being  
34             appropriate for receipt of a conductive lead of an  
35             electronic component.

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37        4. Structure as in Claim 3 wherein the interior  
38             surface of each hole is plated with a conductive material.

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2       5. Structure as in Claim 4 wherein the conductive  
3 material on the interior of each hole is electrically  
4 connected to a corresponding one of said electrically  
5 conductive traces.  
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7       6. Structure as in Claim 1 including a multiplicity  
8 of electronic components mounted on said printed circuit  
9 board, each electrical lead of said electronic components  
10 each making contact with a corresponding electrical contact  
11 selected from said plurality of electrical contacts.  
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13       7. Structure as in Claim 6 wherein said at least one  
14 integrated circuit chip comprises one integrated circuit  
15 chip.  
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17       8. Structure as in Claim 1 wherein at least some of  
18 said electrical contacts on said printed circuit board  
19 comprise pads, each pad being connected to a corresponding  
20 one of said plurality of electrically conductive traces  
21 formed on said printed circuit board.  
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23       9. Structure as in Claim 8 wherein each pad is  
24 connected by a conductive lead to a hole formed through said  
25 printed circuit board, said hole being plated on its  
26 interior surface by a conductive material and said hole  
27 being in electrical contact with a corresponding one of said  
28 electrically conductive traces formed on said printed  
29 circuit board.  
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31       10. Structure as in Claim 1 wherein said printed  
32 circuit board comprises:  
33              a first portion thereof containing conductive  
34              traces for interconnecting electronic components formed  
35              thereon without the use of a programmable integrated  
36              circuit; and  
37              a second portion thereof containing at least one  
38              programmable integrated circuit for interconnecting

1        electronic components formed on at least said second  
2        portion of said printed circuit board.  
3

4        11. A printed circuit board comprising:

5              a multiplicity of first electrical contacts formed  
6        in said printed circuit board for receipt of the leads  
7        of electronic components to be mounted on said printed  
8        circuit board;

9              a corresponding multiplicity of second electrical  
10       contacts formed in a selected region of said printed  
11       circuit board for receipt of the leads on at least one  
12       package of at least one integrated circuit chip to be  
13       mounted on the printed circuit board for use in  
14       interconnecting selected ones of said multiplicity of  
15       first electrical contacts; and

16              conductive traces formed on said printed circuit  
17       board, each conductive trace uniquely interconnecting  
18       one first electrical contact to a corresponding second  
19       electrical contact.

20        12. A printed circuit board as in Claim 11 including  
21       at least one integrated circuit mounted thereon wherein said  
22       at least one integrated circuit comprises a programmable  
23       circuit for interconnecting selected conductive traces  
24       formed on said printed circuit board thereby to form the  
25       electronic components to be contained thereon into a  
26       selected electrical circuit.  
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28        13. Structure as in Claim 12 including means for  
29       testing the state of said at least one programmable  
30       integrated circuit to determine the state of the signals on  
31       said conductive traces.  
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33        14. Structure as in Claim 13 including means for  
34       transmitting control signals to said at least one integrated  
35       circuit for controlling the configuration of said at least  
36       one integrated circuit so as to control the interconnection  
37       of the conductive traces formed on said printed circuit  
38

board.

15. Structure as in Claim 14 including at least one programmable integrated circuit mounted on said printed circuit board for interconnecting selected traces formed on said printed circuit board.

16. Structure as in Claim 15 wherein said printed circuit board comprises:

a first portion thereof containing conductive traces for interconnecting electronic components formed thereon without the use of a programmable integrated circuit; and

a second portion thereof containing at least one programmable integrated circuit for interconnecting electronic components formed on at least said second portion of said printed circuit board.

17. A printed circuit board comprising:

a multiplicity of component holes for receipt of leads of electronic components;

a corresponding multiplicity of PIC holes for receipt of the leads on the package or packages of a programmable interconnect chip or chips; and

one or more layers of conductive traces formed on said printed circuit board, each conductive trace uniquely connecting one component hole to one PIC hole.

18. Structure as in Claim 17 wherein said printed circuit board comprises:

a first portion thereof containing conductive traces for interconnecting electronic components formed thereon without the use of a programmable integrated circuit; and

a second portion thereof containing at least one programmable integrated circuit for interconnecting electronic components formed on at least said second portion of said printed circuit board.

1       19. The method of configuring an electronic system on  
2 a printed circuit board comprising the steps of:

3             creating a computer model of the programmable PC  
4 board containing a plurality of component contacts for  
5 receipt of the leads of electronic components to be  
6 mounted on said printed circuit board, a corresponding  
7 plurality of PIC contacts for receipt of the leads of  
8 one or more programmable interconnect chips ("PIC") for  
9 use in interconnecting selected electronic components  
10 and conductive traces, each conductive trace connecting  
11 one component contact to one PIC contact;

12             simulating the placement and routing of select  
13 electronic components on the component contacts;

14             simulating the electrical performance of the  
15 system with the electrical components interconnected by  
16 the PIC;

17             interconnecting the electronic components in a  
18 desired fashion by configuring the PIC to achieve such  
19 interconnection;

20             determining the system performance and system  
21 characteristics with the electronic components so  
22 interconnected by simulating and/or testing the system  
23 so interconnected; and

24             repeating the above steps making those changes in  
25 placement of electronic components as indicated to be  
26 required by the simulation or test results until the  
27 above steps yield an electronic system which yields the  
28 desired characteristics and functional performance.

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30       20. A programmable interconnect chip for use in  
31 interconnecting electronic components formed on a printed  
32 circuit board, said chip comprising:

33             a first set of conductive leads formed in a first  
34 direction across the surface of said chip, each of said  
35 conductive leads comprising one or more conductive  
36 segments, portions of selected ones of said segments  
37 being connected to pads on the surface of said

1       programmable interconnect chip, each of said pads being  
2       adapted for contact to a corresponding contact on the  
3       printed circuit board;

4              a second set of conductors formed on said  
5       programmable interconnect chip in a second direction  
6       not parallel to said first direction, each conductive  
7       lead in said second set of conductive leads comprising  
8       one or more segments; and

9              means for electrically interconnecting selected  
10      ones of said conductive leads in said first set of  
11      conductive leads to one or more of said conductive  
12      leads in said second set of conductive leads.

13       21. Structure as in Claim 20 wherein said programmable  
14      interconnect chip comprises:

15              active transistor in said programmable  
16      interconnect chip;

17              means for electrically connecting selected ones of  
18      the segments of conductive leads in said first set of  
19      conductive leads and in said second set of conductive  
20      leads to programmable transistors in the substrate of  
21      said programmable interconnect chip; and

22              means for programming said programmable  
23      transistors in said interconnect chip so as to turn on  
24      selected ones of the transistors in said programmable  
25      interconnect chip to form desired interconnections  
26      between selected contacts on said printed circuit  
27      board.

28       22. Structure as in Claim 20 wherein said means for  
29      electrically interconnecting comprise a plurality of  
30      interconnect structures, each interconnect structure  
31      comprising:

32              a first conductive layer comprising a portion of  
33      the conductive segment of a conductive lead in said  
34      first set of leads;

35              a second conductive layer comprising a portion of  
36      the conductive segment of a conductive lead in said  
37      leads;

1       second set of conductive leads; and  
2           dielectric formed between said first conductive  
3           lead and said second conductive lead, said dielectric  
4           being capable of being made conductive by the  
5           application of a selected voltage thereto, thereby to  
6           form an electrically conductive path from said  
7           conductive segment in said first set of conductive  
8           leads to said conductive segment in said second set of  
9           conductive leads.

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